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10/581,873	06/05/2006	Tim Niggemeier	PD030127	3929
<sup>24498</sup> Joseph J. Laks	7590 10/02/200	EXAMINER		
Thomson Licen		GIARDINO JR, MARK A		
PO Box 5312	Way, Patent Operation	ART UNIT	PAPER NUMBER	
PRINCETON, 1	NJ 08543	2185		
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			10/02/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary		Applicat	Application No. Appli		olicant(s)	
		10/581,8	73	NIGGEMEIER ET AL.		
		Examine	r	Art Unit		
			GIARDINO JR	2185		
<i> Th</i> Period for Re	e MAILING DATE of this communic eply	cation appears on th	e cover sheet with the	e correspondence a	ddress	
WHICHEN - Extensions after SIX (6 - If NO perio - Failure to n Any reply n	FENED STATUTORY PERIOD FO /ER IS LONGER, FROM THE MA of time may be available under the provisions of i) MONTHS from the mailing date of this commu- d for reply is specified above, the maximum state pely within the set or extended period for reply ve- eceived by the Office later than three months affent term adjustment. See 37 CFR 1.704(b).	AILING DATE OF T of 37 CFR 1.136(a). In no e- unication. tutory period will apply and v vill, by statute, cause the ap	HIS COMMUNICATION  vent, however, may a reply be  vill expire SIX (6) MONTHS from  plication to become ABANDO	ON. timely filed om the mailing date of this NED (35 U.S.C. § 133).	·	
Status						
2a)⊠ This 3)⊡ Sind	sponsive to communication(s) filed is action is <b>FINAL</b> . 2 ce this application is in condition fixed in accordance with the practic	b)∏ This action is of allowance excep	t for formal matters, ¡		e merits is	
Disposition o	of Claims					
4a) 0 5)	im(s) <u>1-14</u> is/are pending in the ap Of the above claim(s) is/are im(s) is/are allowed. im(s) <u>1-14</u> is/are rejected. im(s) is/are objected to. im(s) are subject to restrict	e withdrawn from co				
Application F	Papers					
10)☐ The App Rep	specification is objected to by the drawing(s) filed on is/are: licant may not request that any object lacement drawing sheet(s) including oath or declaration is objected to	a) accepted or b tion to the drawing(s) the correction is requi	be held in abeyance. Since if the drawing(s) is	See 37 CFR 1.85(a). objected to. See 37 C	, ,	
Priority unde	er 35 U.S.C. § 119					
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>						
2) Notice of D 3) Information	References Cited (PTO-892) Draftsperson's Patent Drawing Review (PT n Disclosure Statement(s) (PTO/SB/08) s)/Mail Date	ГО-948)	4) Interview Summa Paper No(s)/Mail 5) Notice of Informa 6) Other:	Date		

#### **DETAILED ACTION**

The Examiner acknowledges the applicant's submission of the amendment dated 6/23/2008. At this point claims 1, 3, 13, and 14 have been amended and no claims have been added or canceled. Thus, claims 1-14 are pending in the instant application.

The instant application having Application No. 10/581,873 has a total of 14 claims pending in the application, there are 2 independent claims and 12 dependent claims, all of which are ready for examination by the examiner.

#### **REJECTIONS BASED ON PRIOR ART**

# Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 10, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Chauvel et al (US 6,412,048).

Regarding Claim 1, Chauvel teaches a method for communication between an IC (host 12) and an external DRAM (SDRAM 24), where the external DRAM has at least one memory bank (see description of how the memory is arranged into banks on Column 6 Lines 33-40) and communicates with the IC via two or more channels, wherein the transmission of memory bank commands of multiple channels (see Column

15 Lines 19-24 and Table 2 on Column 15 for a list of channels) is prioritized on the basis of a static priority allocation for commands (see the state machine of Figure 4, read/write in steps 49 and 64, deactivate in steps 54 and 68, and activate in steps 56 and 70 have specific and static places in the memory controller) and a dynamic priority allocation for the channels (Column 15 Lines 19-24, also see Table 2 on Column 15 for a list of channels).

Regarding Claim 5, Chauvel teaches all limitations of Claim 1, wherein the dynamic priority allocation involves one of the channels losing the highest priority only when it can send a command (see Column 17 Lines 14-30, note that after a command has been sent the peripheral device gains priority over time and reverts back to normal priority when it can again send a command, also see Column 16 Lines 9-11, which indicates that each channel may not have multiple requests pending).

Regarding Claim 10, Chauvel teaches all limitations of Claim 1, wherein two successive access operations to a memory bank are permitted when they are made to the same row in the memory bank (see Figure 4 and particularly steps 46 and 58, where if two successive requests are made to the same row in the memory bank they are permitted).

**Claim 13** is the memory controller with the same limitations as Claim 1, and is rejected on the same grounds.

Claim 14 is the appliance for reading and/or writing to storage media with the same limitations of Claim 1, and is rejected on the same grounds.

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#### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Kirsch (US 2004/0054844). Chauvel teaches all limitations of Claim 1 as described above. In addition, Chauvel teaches a Read or Write command having the highest priority, since neither an Activate nor a Precharge command is given unless a read or write is present (see Figure 4 in Chauvel). The Activate command is given next highest priority, since a Precharge command is only run if a new row in the bank must be activated. However, though Chauvel makes references to a burst terminate type command (see STOP command on Table 1 and DMA Burst Req size signal on Table 4), Chauvel does not say what kind of priority is given to such commands. Kirsch teaches a burst terminate command takes precedence over write and read commands (see how the burst terminate command resets the state machine to the active state in Figure 7, also see paragraph 0071 in Kirsch). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the burst terminate command as a higher priority command than read or write. This would be useful when a separate read or write request must be taken care of while the memory is in the middle of a lengthy burst

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(Chauvel mentions a scenario like this in Column 21 Lines 41-49, and though his solution is different, combining the two devices as described is another solution to the problem).

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Jones et al (US 6,301,642). Regarding Claim 3, Chauvel teaches all limitations of Claim 1 as described above. However, he does not teach a channel being given the lowest priority after a command has been sent. Jones teaches a round robin style memory arbiter (Column 1 Lines 51-62 in Jones). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this style for the channels instead of the way described by Chauvel, since in some embodiments each channel may have equal rights to access the memory, and the round robin memory arbiter allows for fairer access than assigned priorities for each channel.

This combined device meets all limitations of Claim 4, since Chauvel meets all limitations of Claim 1, wherein the dynamic priority allocation involves one of the channels being given highest priority in the next clock cycle if it does not have the highest priority in the current clock cycle and another channel sends a command (see Column 1 Lines 51-62 in Jones, if the channel with highest priority sends a command a different channel will have highest priority on the next clock cycle, also see Column 16 Lines 9-11, which indicates that each channel may not have multiple requests pending).

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Wheeler et al (US 6,983,350). Regarding Claim 7, Chauvel teaches all limitations of Claim 1 as described above, as well as channels sharing the SDRAM resource (note Figure 4, where the next pending request, which could be from a different channel, is observed to see if it is on the same row, indicating joint use, also see Column 16 Lines 9-11 in Chauvel, which indicates that each channel may not have multiple requests pending). However, Chauvel does not teach giving no successive access operations to a jointly used memory bank. Wheeler teaches alternating memory banks such that no successive access operation accesses a jointly used memory bank (Column 5 Lines 33 to 42 in Wheeler). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to arrange memory operations in such a way. Wheeler provides the motivation when he states that the bandwidth of the RAM is improved (Column 5 Lines 40-42 in Wheeler).

This combined device meets all limitations of Claim 9, since Chauvel meets all limitations of Claim 1, wherein two access operations to a memory bank always have an access operation to another memory bank effected between them (Column 5 Lines 33 to 42 in Wheeler, alternating between an even and odd memory bank places at least one access operation between each bank).

Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Chen et al (US 2003/0051108). Regarding Claim 8, Chauvel

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teaches all limitations of Claim 1 As described above. However, Chauvel does not teach a network provided which allows at least one channel to access various memory banks. Chen teaches a network (Bank Usage Sorter 110 in Chen) that allows the channels to access any memory bank (paragraph 0014, also see Figure 3 in Chen). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this network to distribute the memory data evenly across the banks because this reduces costs (see Paragraph 0015 in Chen).

Note that this device meets all limitations of Claim 6, since the channels are accessing physically separate memory areas (banks WO – W7 in Chen) in the external DRAM.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of LaBerge (US 2001/0044885). Chauvel teaches all limitations of Claim 1 as described above. However, Chauvel is silent on the details of how the memory bank works. LaBerge teaches a memory bank that has a state machine (containing at least the states 'idle' and 'not idle', see Paragraph 0023 and Figure 8 in LaBerge). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used a state machine to control the memory banks because tracking idle states results in reducing latency incurred between successive memory operations (see Paragraph 0019 in LaBerge).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of the power point entitled "Random Access Memory". Chauvel teaches all limitations of Claim 1 as described above. However, Chauvel does not teach the composition of the DRAM memory. "Random Access Memory" teaches combining several RAM modules into a single RAM module and a chip enable signal (called chip select in the power point) to select the desired module (see Slides 17 and 18). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have combined the RAM modules this way because it allows for larger memories to be made (see Slide 18 in "Random Access Memory").

# ARGUMENTS CONCERNING NON-PRIOR ART REJECTIONS/OBJECTIONS <u>Drawing Objections</u>

Applicant's arguments/amendments with respect to the drawings have been considered and have overcome the Examiner's prior objections and thus are withdrawn.

## **Specification Objections**

Applicant's arguments/amendments with respect to the specification have been considered and have overcome the Examiner's prior objections and thus are withdrawn.

# Claim Objections

Applicant's amendment with respect to the objection of claim 3 has been considered and has overcome the Examiner's prior objection and thus is withdrawn.

Applicant's amendment with respect to claim 5 has been considered and has overcome the Examiner's prior rejection and thus is withdrawn.

## **ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

## Rejections - USC 102/103

Applicant's arguments with respect to claims 1 and 13 have been considered but are not persuasive. While Chauvel may teach the commands transmitted in order within given channels, Chauvel still teaches all limitations of Claim 1 in the broadest reasonable interpretation.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (specifically, taking into account the specific command and from which channel the command came from, and subsequently prioritizing the commands from all channels) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's argument with respect to Claim 2 that Chauvel does not teach the features of Claim 1 has been considered but is not persuasive, as has been discussed in the previous paragraph.

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# **CLOSING COMMENTS**

## **Conclusion**

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

#### STATUS OF CLAIMS IN THE APPLICATION

#### **CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1-14 have received a second action on the merits and are subject of a second action final.

#### <u>DIRECTION OF FUTURE CORRESPONDENCES</u>

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner Art Unit 2185

October 4, 2008

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185